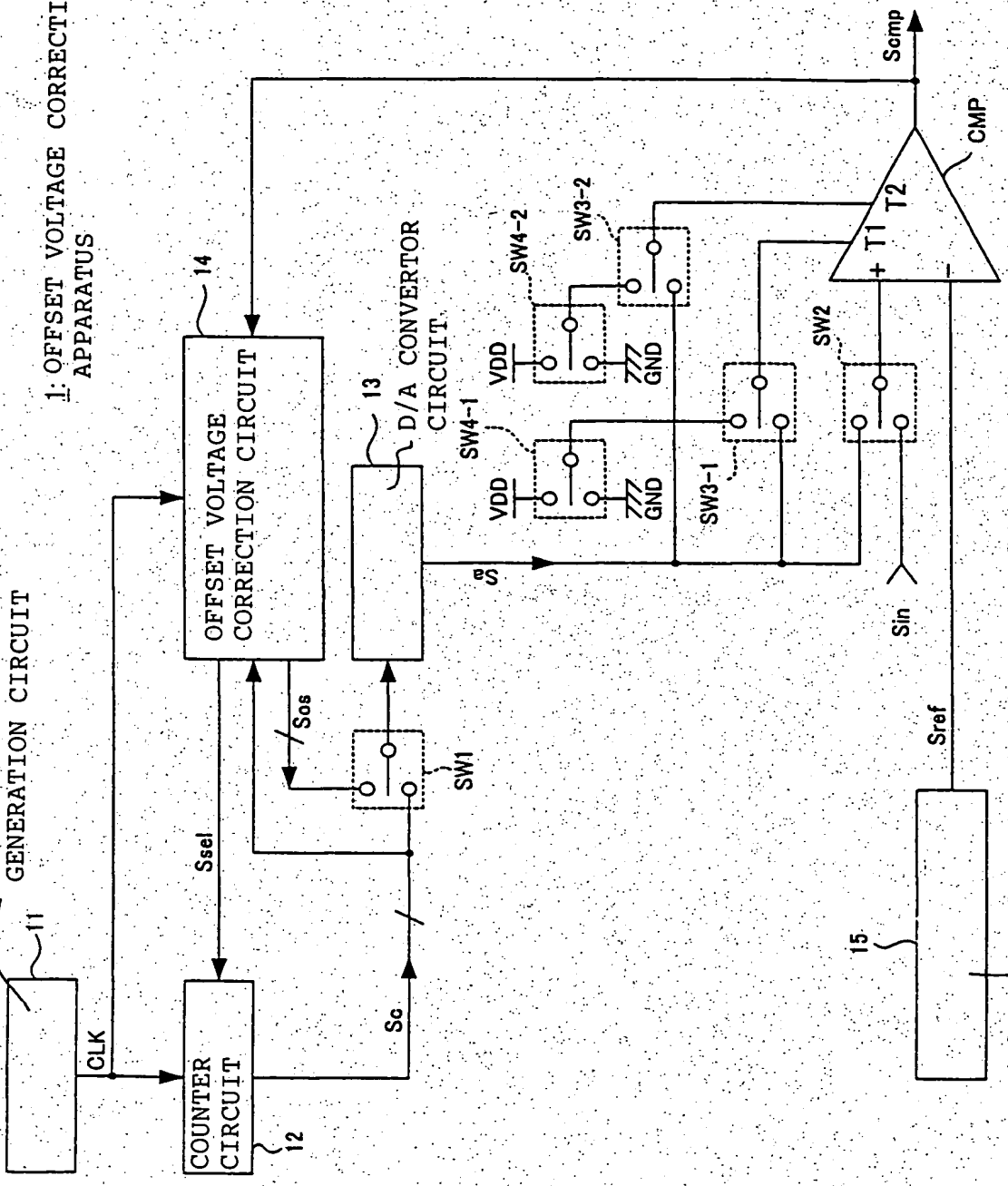
1: OFFSET VOLTAGE CORRECTION APPARATUS
CLOCK SIGNAL GENERATION CIRCUIT
11
CLK
COUNTER CIRCUIT
12
Ssel
Sc
Sos
SW1
OFFSET VOLTAGE CORRECTION CIRCUIT
14
13
D/A CONVERTOR CIRCUIT
Ss
SW4-1
SW4-2
SW3-1
SW3-2
SW2
VDD
GND
Samp
CMP
T1
T2
+
-
Sin
Sref
15
REFERENCE VOLTAGE GENERATION CIRCUIT

FIG. 1

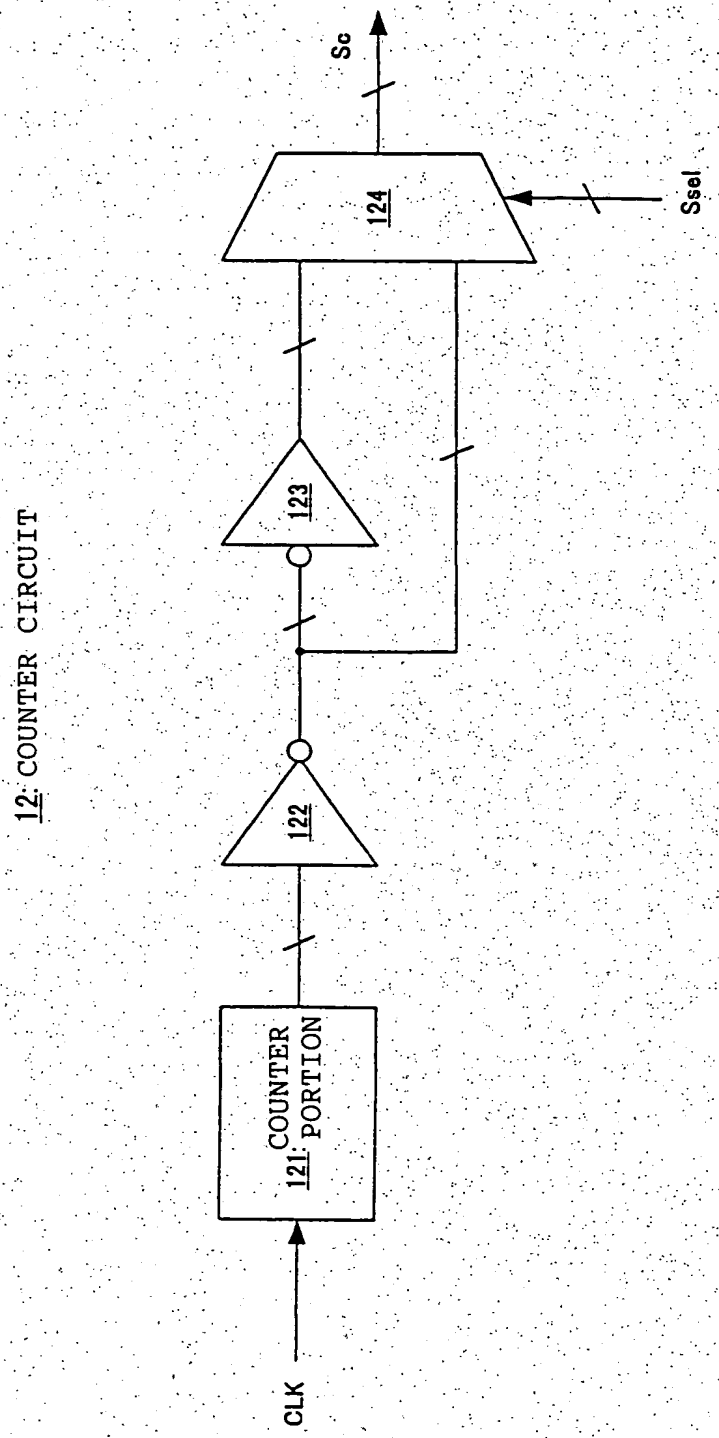
12: COUNTER CIRCUIT
CLK
121: COUNTER PORTION
122
123
124
Ssel
Sc

FIG. 2

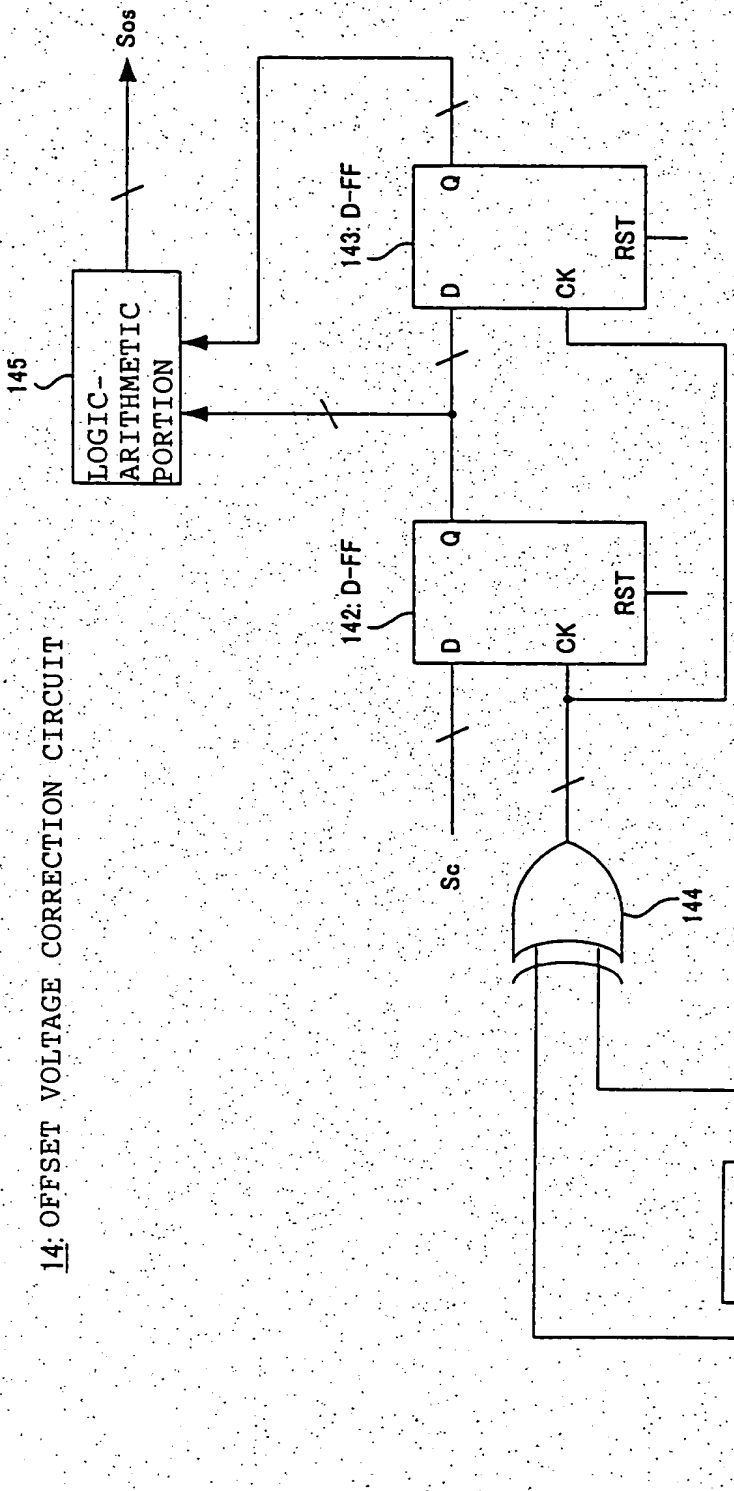
14: OFFSET VOLTAGE CORRECTION CIRCUIT
Sos
145
LOGIC-ARITHMETIC PORTION
143: D-FF
142: D-FF
141: D-FF
144
Sc
Scmp
CLK
D
Q
CK
RST

FIG.3

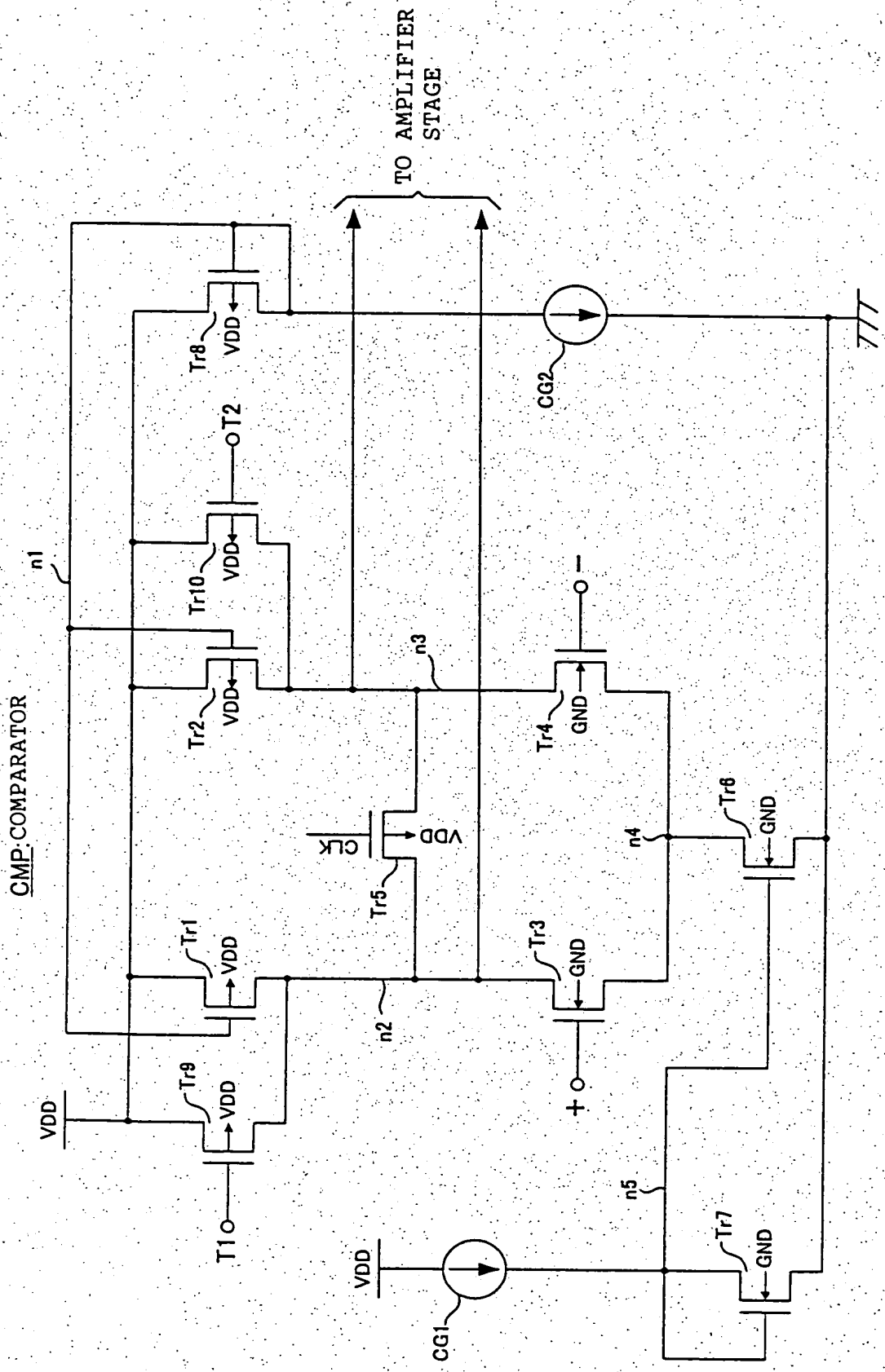
CMP:COMPARATOR
TO AMPLIFIER STAGE
VDD
GND
CLK
T1
T2
Tr1
Tr2
Tr3
Tr4
Tr5
Tr6
Tr7
Tr8
Tr9
Tr10
CG1
CG2
n1
n2
n3
n4
n5
+
-

FIG. 4

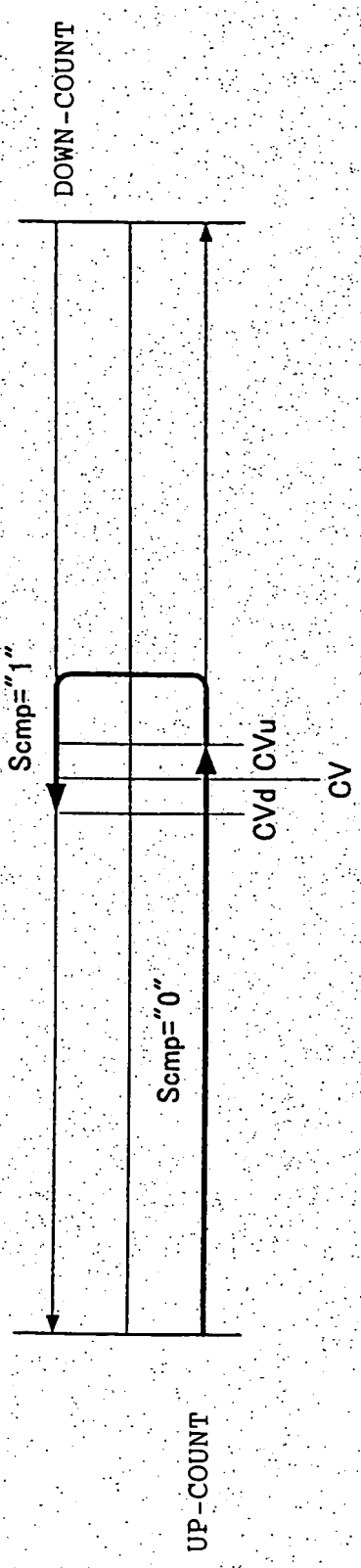

FIG.5

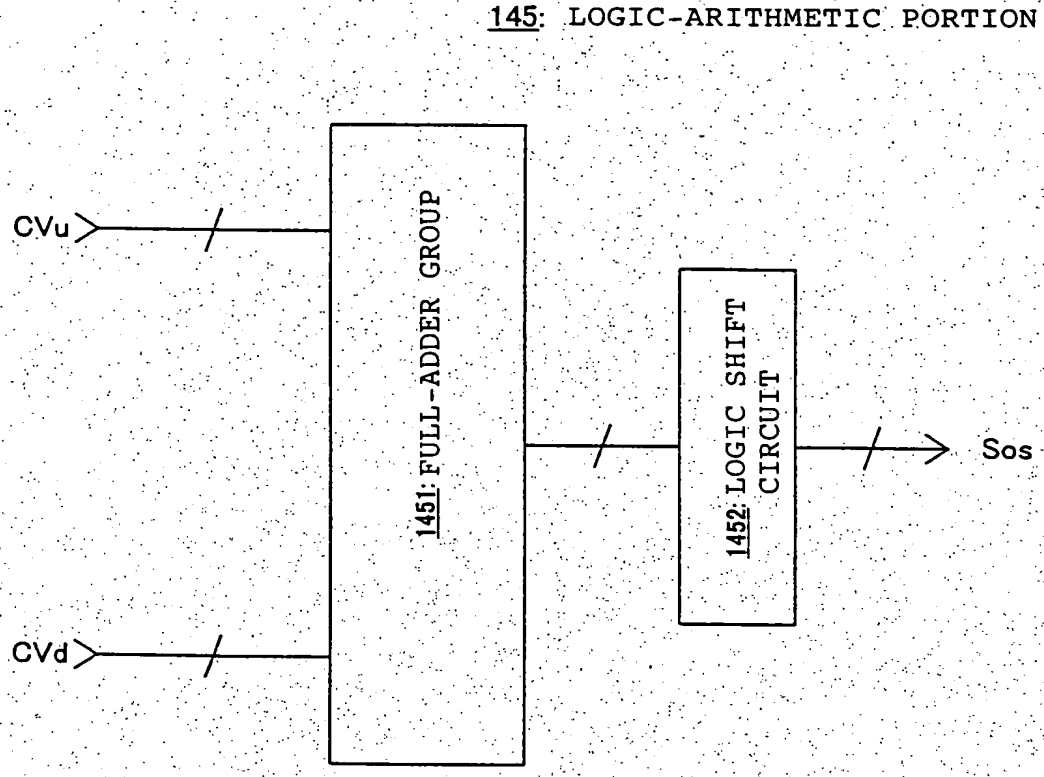
145: LOGIC-ARITHMETIC PORTION
CVu
CVd
1451: FULL-ADDER GROUP
1452: LOGIC SHIFT CIRCUIT
Sos

FIG. 6

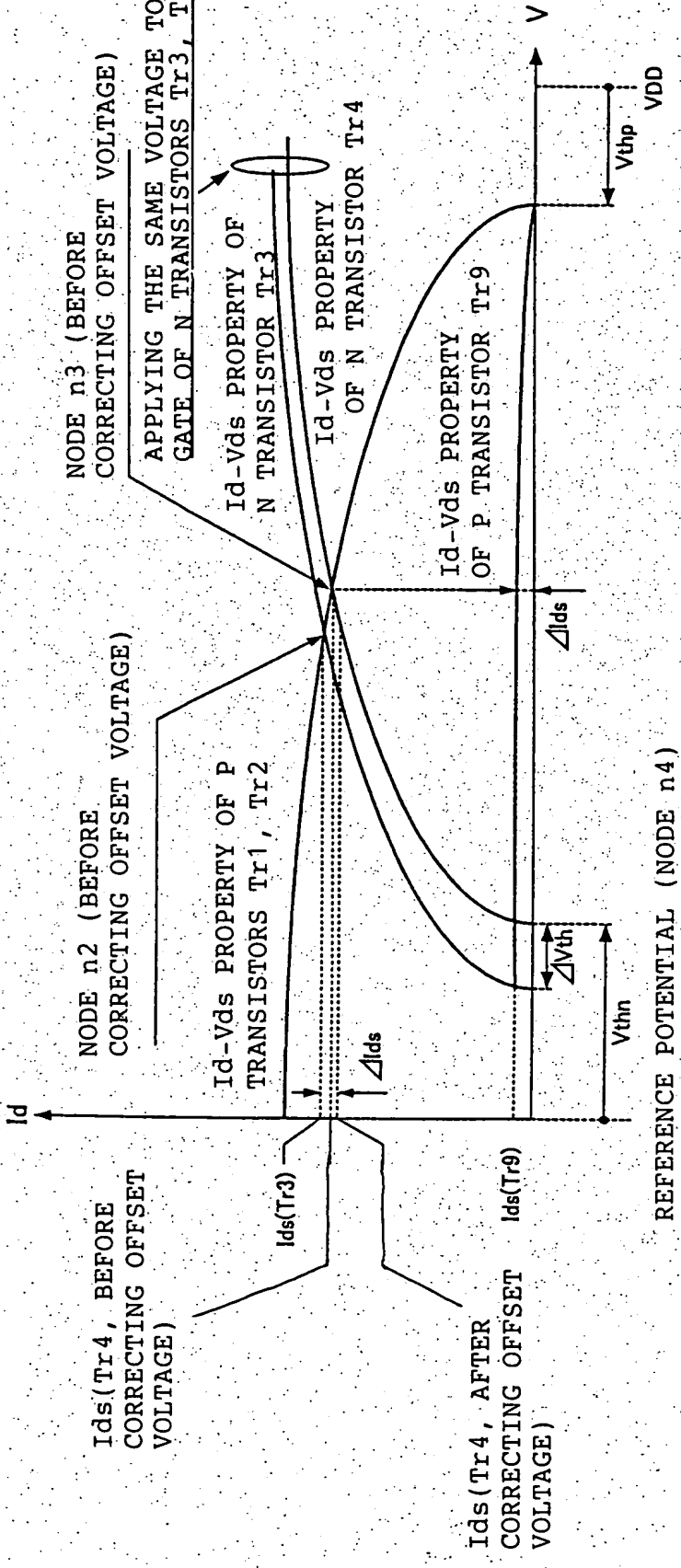
Id
V
NODE n3 (BEFORE CORRECTING OFFSET VOLTAGE)
APPLYING THE SAME VOLTAGE TO THE GATE OF N TRANSISTORS Tr3, Tr4
Id-Vds PROPERTY OF N TRANSISTOR Tr3
Id-Vds PROPERTY OF N TRANSISTOR Tr4
Id-Vds PROPERTY OF P TRANSISTOR Tr9
NODE n2 (BEFORE CORRECTING OFFSET VOLTAGE)
Id-Vds PROPERTY OF P TRANSISTORS Tr1, Tr2
Vthp
VDD
Δids
Δids
Δvth
Vthn
Ids(Tr3)
Ids(Tr9)
Ids(Tr4, BEFORE CORRECTING OFFSET VOLTAGE)
Ids(Tr4, AFTER CORRECTING OFFSET VOLTAGE)
REFERENCE POTENTIAL (NODE n4)

FIG. 7

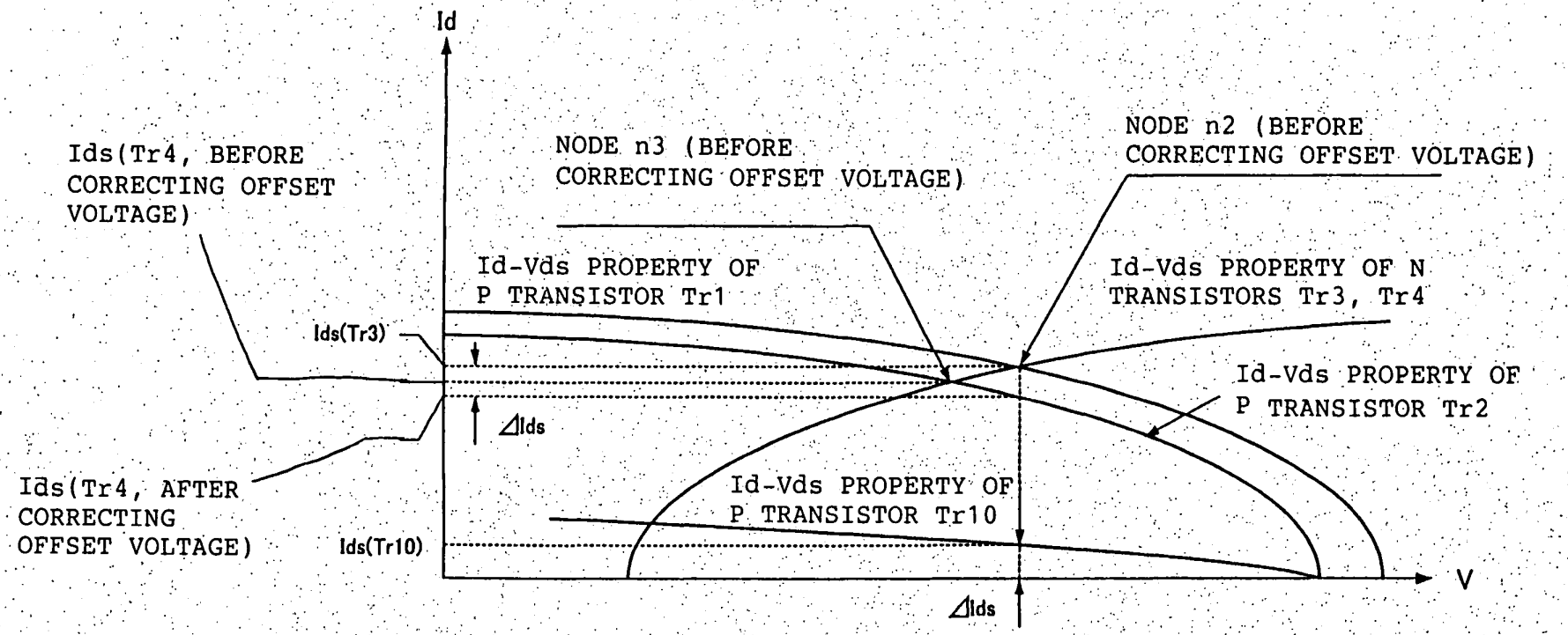
Id
Ids(Tr4, BEFORE CORRECTING OFFSET VOLTAGE)
NODE n3 (BEFORE CORRECTING OFFSET VOLTAGE)
NODE n2 (BEFORE CORRECTING OFFSET VOLTAGE)
Id-Vds PROPERTY OF P TRANSISTOR Tr1
Id-Vds PROPERTY OF N TRANSISTORS Tr3, Tr4
Ids(Tr3)
Id-Vds PROPERTY OF P TRANSISTOR Tr2
⊿Ids
Ids(Tr4, AFTER CORRECTING OFFSET VOLTAGE)
Id-Vds PROPERTY OF P TRANSISTOR Tr10
Ids(Tr10)
V
⊿Ids

FIG. 8

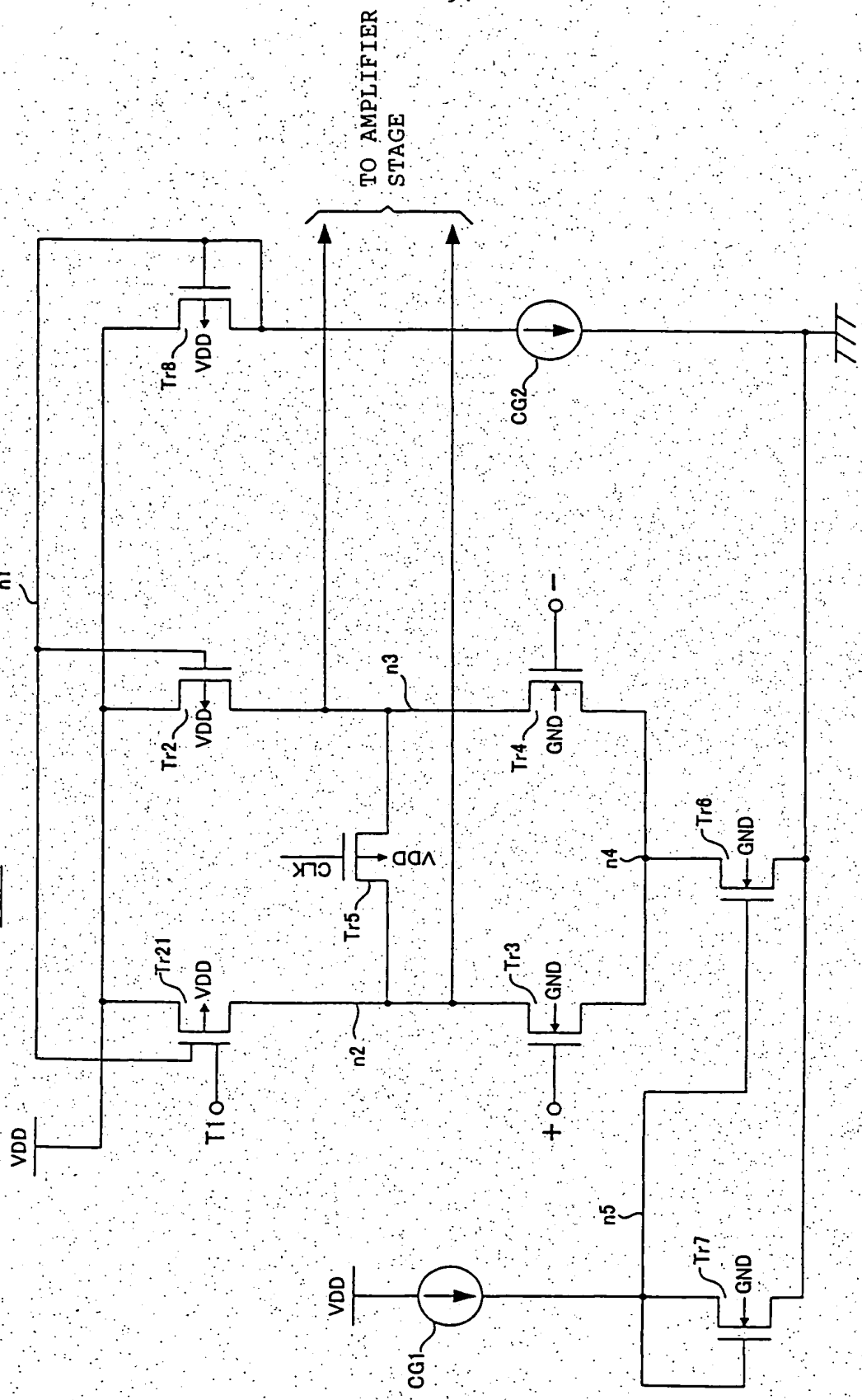
CMP2: COMPARATOR
TO AMPLIFIER STAGE
VDD
T1
Tr21
Tr2
Tr8
Tr3
Tr4
Tr5
Tr6
Tr7
CLK
GND
CG1
CG2
n1
n2
n3
n4
n5

FIG. 9

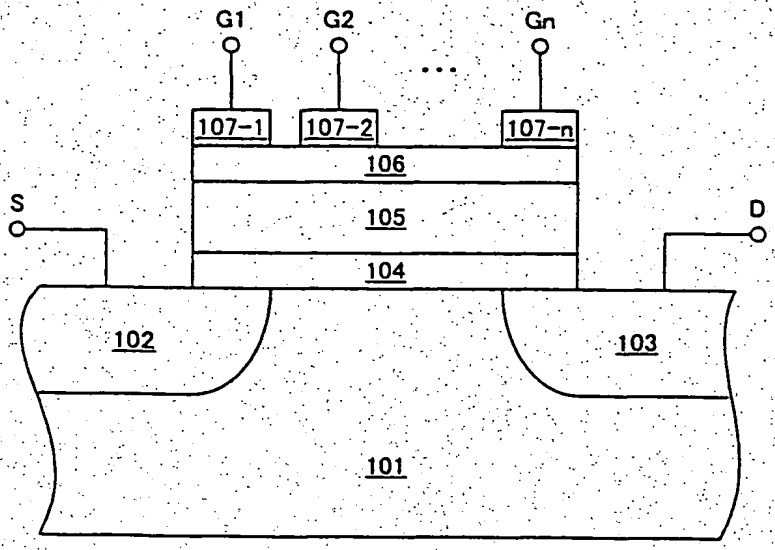

FIG. 10

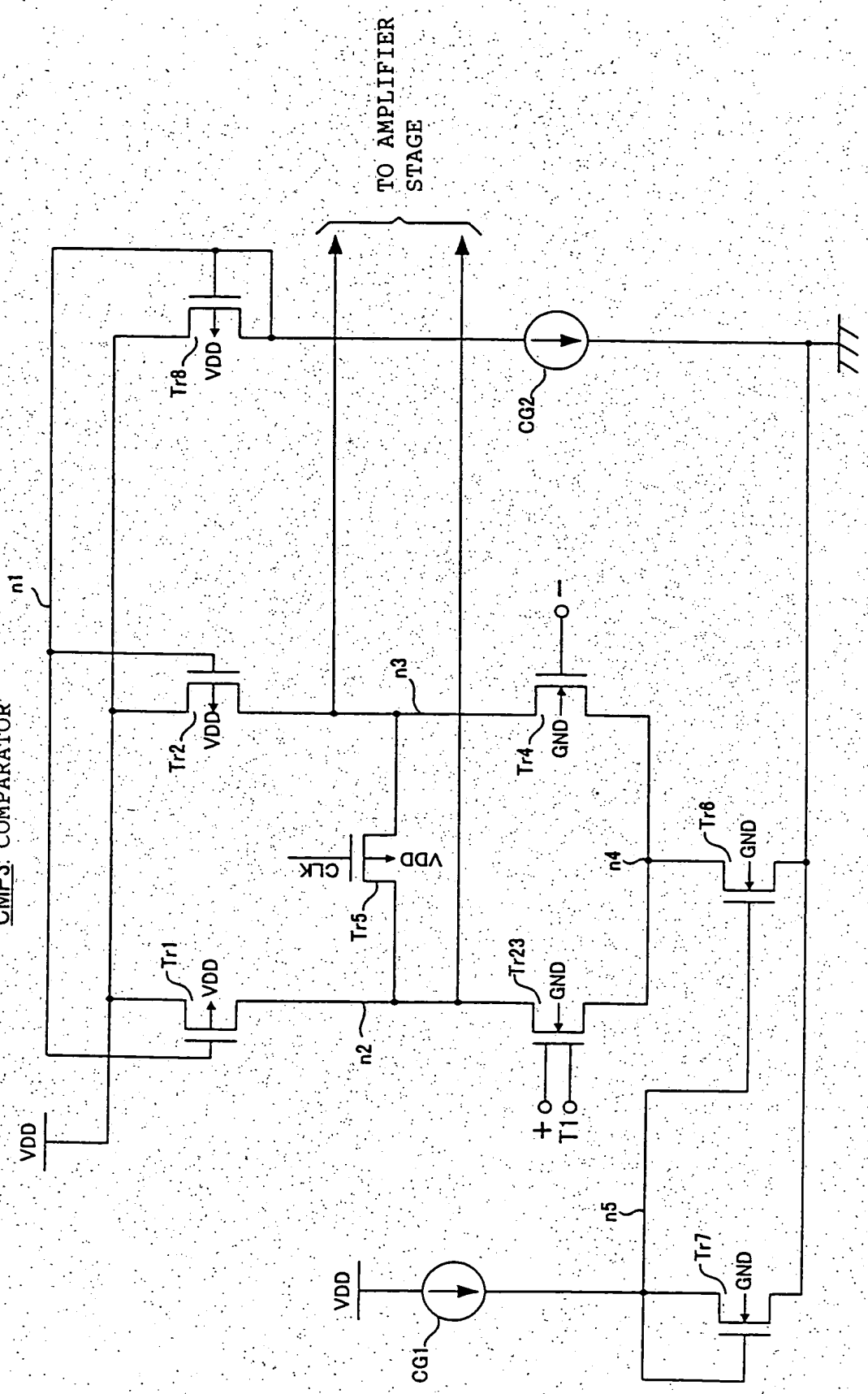
TO AMPLIFIER STAGE
CMP3: COMPARATOR
n1
n2
n3
n4
n5
Tr1
Tr2
Tr4
Tr5
Tr6
Tr7
Tr8
Tr23
VDD
GND
CLK
CG1
CG2
T1
+
-

FIG. 11